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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/784,114	02/20/2004	Kelly Cameron	51798/RJP/B600	5258

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EXAMINER

TORRES, JOSEPH D

ART UNIT PAPER NUMBER

2133

DATE MAILED: 03/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/784,114

Applicant(s)

CAMERON, KELLY

Examiner

Joseph D. Torres

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 1 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 09 November 2004.
- 2a) ☐ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 2-21 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☐ Claim(s) \_\_\_\_\_ is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☒ Claim(s) 2-21 are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☒ Interview Summary (PTO-413)  
Paper No(s)/Mail Date 20050301.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Election/Restrictions*

Restriction to one of the following inventions is required under 35 U.S.C. 121:

- I. Claims 2-13, drawn to a memory array having a plurality of array cells, M, with selected array cells storing symbols therein, the memory array having a memory block length, N and an interleave depth, D; wherein the memory array includes a plurality of interleaver array rows, the plurality of interleaver array rows including a selected row,  $R_i$ , having a row length, S, determined by:  $S = \lfloor ((D-1)/N)R_i \rfloor + 1$ , classified in class 714, subclass 788.
- II. Claims 14-18, drawn to a memory array having a plurality of array cells, M, with selected array cells storing symbols therein, the memory array having a memory block length, N and an interleave depth, D; wherein one of the read commutator and the write commutator changes position using a predetermined modulo technique, the predetermined modulo technique incrementing the position of the one of the read commutator and the write commutator by rows, wherein K and K satisfies:  $KD \bmod N \equiv 1$ , classified in class 714, subclass 702.
- III. Claims 19-21, drawn to a memory array having a plurality of array cells, M, with selected array cells storing symbols therein, the memory array having

a memory block length, N and an interleave depth, D; wherein the memory array includes a plurality of interleaver array rows, the plurality of interleaver array rows including a selected row,  $R_i$ , having a role length, S, determined by:  $U = \lfloor ((D-1)/N)(N-1-R_d) \rfloor + 1$ , classified in class 714, subclass 788.

The inventions are distinct, each from the other because of the following reasons:

Inventions Group I, Group II and Group III are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention Group I has separate utility such as for interleaving wherein the memory array includes a plurality of interleaver array rows, the plurality of interleaver array rows including a selected row,  $R_i$ , having a role length, S, determined by:  $S = \lfloor ((D-1)/N)R_i \rfloor + 1$ . In the instant case, invention Group II has separate utility such as in memory access wherein one of the read commutator and the write commutator changes position using a predetermined modulo technique, the predetermined modulo technique incrementing the position of the one of the read commutator and the write commutator by rows, wherein K and K satisfies:  $KD \bmod N \equiv 1$ . In the instant case, invention Group III has separate utility such as for de-interleaving wherein the memory array includes a plurality of interleaver array rows, the plurality of interleaver array rows including a selected row,

$R_i$ , having a role length,  $S$ , determined by:  $U = \lfloor ((D-1)/N)(N-1-R_d) \rfloor + 1$ . See MPEP

§ 806.05(d).

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search required for Group I-III is mutually exclusive, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art because of their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

A telephone call was made to Peter C. Hsueh on 2/28/2005 to request an oral election to the above restriction requirement, but did not result in an election being made.

Applicant is advised that the reply to this requirement to be complete must include an election of the invention to be examined even though the requirement be traversed (37 CFR 1.143).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (571) 272-3829. The examiner can normally be reached on M-F 8-5.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Joseph D. Torres, PhD  
Primary Examiner  
Art Unit 2133

